Society for Electronic Transactions and Security [SETS], Chennai, India

Advertisement for the Post of RA and JRFs in DST funded project

Date: 10th May, 2019

SETS invites applications from citizens of India for filling up the positions of **Research Associate** and **JRF** for a sponsored project from **Department of Science and Technology (DST), Government of India** to SETS for 3 years.

Title of the Sponsored Project: *Design and Development of Fast and Robust Authentication and Key Distillation Protocols for QKD systems*

Short description of the research project: Quantum Key Distribution (QKD) is a cryptographic method which enables two or more parties to establish a shared secret key between them. The main bottleneck in making high speed QKD is the post-processing phase that run on a classical channel which is very inefficient when compared to the rate at which raw key is generated from the quantum channel. Thus, the post-processing received much attention in the recent years in order to improve the final QKD key rate. In this project, the main goal is to develop new and efficient modules for data acquisition and processing required for fibre-based and free-space QKD systems. In particular, the deliverable will be a QKD post-processing engine running on FPGAs. The post-processing engine will feature modules for sifting, parameter estimation, synchronization, authentication, privacy amplification, error correction and verification.

Key Functions and Responsibilities for all the posts:

- Work with components for QKD system development
- Realize complex FPGA design from specifications to board integration (Specification, FPGA synthesis, design, validation and integration of the FPGA devices)
- Ensure functional tests of FPGA's on developed boards and demonstrate to subject matter experts
- Work with core project group and subject matter experts

Post 1: Research Associate (Number of Posts: 1)

Duration: 3 years

Salary: Rs 47000 p.m. plus 24% HRA

Essential Qualifications: a) PhD in Engineering/Science in the relevant area of the project or b) M.E/M.Tech in Microelectronics and Photonics/Laser and Electro Optics/Electronics and Communication Engineering/VLSI Design/Digital Electronics/Embedded Systems/ or equivalent from a recognized university with First Class or equivalent with at least 3 years of relevant experience.

Desirable Skills/ Knowledge:

a) Knowledge of Quantum Communication and Information.
b) Hands-on experience in optical communication interfaces.
c) Knowledge of Xilinx FPGA implementation flow and tools.
d) Knowledge of FPGA realization and control softwares.

Selection Procedure: Interview

Post 2: **Junior Research Fellow-JRF** (Number of Posts: 2)

Duration: 3 years

Salary: Rs 31000 p.m. plus 24% HRA

Essential Qualifications: M.E/M.Tech in Electronics and Communication Engineering/Digital Electronics/Embedded Systems/VLSI Design/Microelectronics and Photonics/Laser and Electro Optics/ or equivalent from a recognized university with First Class or equivalent.

Areas of Skill sets/ Knowledge required:

a) Knowledge of Xilinx FPGA implementation flow and tools
b) Hands-on experience in simulation using MATLAB/ModelSim and FPGA realization using VHDL/Verilog programming.
c) Knowledge of clock, memory, DCM, and I/O management and implementation on FPGAs (desirable)
d) Experience in design integration, FPGA I/O communications and testing (desirable)

Selection Procedure: Written Test and Interview

Increment: The positions as proposed are purely temporary on Contract basis with consolidated salary under the project. The contract will be for 3 years. In each year, performance review shall be made to ensure continuation. Upon satisfactory performance, RA will be paid Rs 49000 p.m. plus 24% HRA for the 2nd year and Rs 54000 p.m. plus 24% HRA for the 3rd year. The **JRF** will become **SRF** after two years and will be paid Rs 35000 p.m. plus 24% HRA for the 3rd year. Other rules apply as per prevailing DST norms.

Application Process:

The candidate is required to send the filled-in Personal Particulars Form (Available in the website) by email to **hrqkd2019@setsindia.net**. Candidate should write "**Application for the post of _____ for QKD Project of DST**" in the subject line of his/her E-mail.

Closing date for applications: June 15, 2019

For more information, contact 044-66632521/66632515 or visit https://setsindia.in/careers